Second Call for Papers

2017 International Symposium on VLSI Design, Automation and Test (2017 VLSI-DAT)

The 2017 International Symposium on VLSI Design, Automation and Test will be held on April 24-27, 2017 at the Ambassador Hotel, Hsinchu, Taiwan. Original, unpublished papers on all aspects of VLSI Design, Automation and Test are solicited, including but not limited to :

DESIGN TOPICS	EDA TOPICS	TEST TOPICS
RF, Analog and Mixed-Signal Circuits	Logic and Architecture Synthesis	Test Generation and Compression
Sensors and Interface Circuits	Physical Design and Verification	Design-for-Testability and BIST
Memory Circuits and Systems	Design for Manufacturability	RF, Analog and Mixed-Signal Test
Biomedical Circuits	Power/Thermal Estimation and Optimization	SOC and System Level Test
Energy-Harvesting and Power Circuits	Design Verification	Silicon Debug and Diagnosis
Ultra Low-Power Circuits and Systems	Modeling and Simulation	3D IC and Interposer-Based IC Test
Digital Circuits and ASIC	Electronic System Level Design	Yield and Reliability Enhancement
Multimedia Processing Design	Hardware-Software Co-Design	On-Chip Monitoring
SoC and NoC Architectures	Machine learning for EDA	Adaptive Test
CPU, DSP and Multicore Architectures	EDA for Microfluidic Biochip	Test Standards
System-in-Package Design	Synthesis for Analog Circuits	Test Data Mining
Communication, Security and Safety Design		Memory Test
Embedded System Software		
Design Using Novel Technologies		

➲ GENERAL INSTRUCTIONS

- Prospective authors must submit a self-contained paper with figures and tables electronically through the conference website **Submit your paper!** by October 16, 2016 23:59 (GMT +0800)
- **The paper can be up to 4 pages.** Any submission exceeding 4 pages in length will be returned immediately without review; submissions lacking necessary details will have a low chance of acceptance.
- In addition to the paper and camera-ready manuscript **CLICK HERE**, the submission should be included with a 80~100 Word ABSTRACT, which will be published in the advance and final program if the paper is accepted.
- VLSI-DAT adopts the DOUBLE BLIND REVIEW process; therefore, **DO NOT reveal** your name(s) or affiliation(s) anywhere in the submitted manuscript for the first paper submission.
- Please review the information on IEEE Intellectual Property Rights before submitting your abstract/paper at http://www.ieee.org/web/publications/rights/index.html

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- **The notices of acceptance will be sent out to authors on December 31, 2016.**
- Any changes on title and author list or withdraw after acceptance must be approved by Technical Program Co-Chairs.
- Each accepted paper must be presented by one of its co-author(s) at the symposium to warrant its publication in the proceedings and the authors are required to complete the Symposium registration and payment before February 28, 2017 23:59 (GMT+0800).
- Presentation of accepted papers at the Symposium must be in English and will be limited to 18 minutes with an additional 2 minutes for Q&A. The final manuscript of all accepted papers will be published as submitted in the proceedings.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplorer database.

➲ STUDENT SUBSIDY MORE INFO

Financial support for attending VLSI-DAT 2017 is available for full-time student presenters living outside of Taiwan, and up to 85% discount for all students in registration fee.

➲ SPECIAL SESSION SUBMISSION

To encourage industry and research institutes to share their experiences on system and product development, 2-page papers on system prototyping and product development are solicited. Submission to this special session should specifically select the paper category of System Prototyping / Product Development to be reviewed separately from the regular submissions.

➲ BEST PAPER AWARD MORE INFO

The two best papers will be selected this year through rigorous evaluation process participated by program committee and session chairs.

➲ IMPORTANT DATES

(Note: All are based on Taiwan time, which is eight hours ahead of Greenwich Mean Time (GMT).)

Paper Submission Deadline	**Oct. 16, 2016**
Notification of Acceptance	Dec. 31, 2016
Final Paper (IEEE compatible version) Submission Deadline	Jan. 31, 2017
Author Registration Deadline	Feb. 28, 2017

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